ABSTRACT OF THE DISCLOSURE

A non-volatile semiconductor memory device according to the present invention has a semiconductor substrate and a memory cell having a floating gate provided through a tunnel insulating layer on the semiconductor substrate, and a control gate provided through an inter-layer insulting layer on said floating gate. The inter-insulating layer includes a silicon oxide layer contiguous to said floating gate, a first silicon nitride layer provided by a CVD method on the silicon oxide layer and a second silicon nitride layer provided on said first silicon nitride layer and having a lower trap density than that of the first silicon nitride layer. The inter-insulating layer may includes a silicon oxide layer contiguous to said floating gate and a silicon oxide layer deposited on said silicon oxide layer and having a quantity of hydrogen content on the order of $10^{19}/cm^3$ or less. The inter-insulating layer also may includes a silicon oxide layer serving as a layer contiguous to at least one of the floating gate and the control gate, and having a lower trap density than that of a silicon nitride layer formed by a CVD method.